a storage device which stores translation and protection table (TPT) entries for virtual to physical address translations, and

a mechanism which flushes individual translation and protection table (TPT) entry stored in the storage device in accordance with a corresponding translation cacheable flag included in the individual translation and protection table (TPT) entry.

17. (Amended) The apparatus as claimed in claim 16, wherein the storage device corresponds to an internal cache for storing said translation and protection table (TPT) entries.

21. A method, comprising:

storing, in a cache of an adapter installed in a host system and provided to interface a switched fabric, translation and protection table (TPT) entries from a host memory for virtual to physical address translations and access validation to the host memory during I/O transactions, each of the TPT entries corresponds to a memory portion of the host memory and comprises at least a translation cacheable flag; and

checking a status of the translation cacheable flag of each one or more selected TPT entries stored in the cache of the adapter to determine whether to discard one or more selected TPT entries from the cache of the adapter.

22. The method as claimed in claim 21, further comprising a step of setting the status of the translation cacheable flag per TPT entry, using an operating system (OS), for enabling the adapter to discard individual TPT entries from the cache.

23. The method as claimed in claim 21, wherein each of the TPT entries represents translation of a single page of a host memory.

24. The method as claimed in claim 21, wherein each of the TPT entries comprises:

protection attributes which control read and write access to a given memory region of the host memory;

said translation cacheable flag which specifies whether the adapter may flush a corresponding translation and protection table (TPT) entry stored in the cache;

a physical page address field which addresses a physical page frame of data entry; and

a memory protection tag which specifies whether the adapter has permission to access the host memory.

25. The method as claimed in claim 21, wherein said protection attributes comprise a Memory Write Enable flag which indicates whether the adapter can write to a page of the host memory; a RDMA Read Enable flag which indicates whether the page can be a source of RDMA Read operation; a RDMA Write Enable flag which indicates whether the page can be a target of RDMA Write operation.

26. An adapter in a host system provided to interface a switched fabric, comprising:

a cache to store translation and protection table (TPT) entries from a host memory for virtual to physical address translations and access validation to the host memory during I/O transactions, each of the TPT entries corresponds to a memory portion of the host memory and comprises at least a translation cacheable flag; and

a mechanism to determine a status of the translation cacheable flag of one or more selected TPT entries stored in the cache, and to discard the one or more selected TPT entries from the cache based on the status of the translation cacheable flag.

27. The adapter as claimed in claim 26, further comprising an operating system (OS) to set the status of the translation cacheable flag per TPT entry for enabling the adapter to discard individual TPT entries from the cache.

28. The adapter as claimed in claim 26, wherein each of the TPT entries represents translation of a single page of a host memory.

29. The adapter as claimed in claim 26, wherein each of the TPT entries comprises:

protection attributes which control read and write access to a given memory region of the host memory;

said translation cacheable flag which specifies whether the adapter may flush a corresponding translation and protection table (TPT) entry stored in the cache;

a physical page address field which addresses a physical page frame of data entry; and

a memory protection tag which specifies whether the adapter has permission to access the host memory.

30. The adapter as claimed in claim 26, wherein said protection attributes comprise a Memory Write Enable flag which indicates whether the adapter can write to a page of the host memory; a RDMA Read Enable flag which indicates whether the page can be a source of RDMA Read operation; a RDMA Write Enable flag which indicates whether the page can be a target of RDMA Write operation.--